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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,753	11/13/2003	Bruce W. McGaughy	10585-019-999	1627

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EXAMINER	
PIERRE LOUIS, ANDRE	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,753	MCGAUGHY ET AL.	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 13 November 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 06/21/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 have been presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2.0 Claims 1-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tcherniaev et al. (U.S. Patent No. 6.577.992), in view of Zhou et al. (U.S. Patent 6,807,520).

2.1 In considering the independent claims 1,2, and 23, Tcherniaev et al. substantially teaches a of simulating a circuit having a hierarchical data structure, in particular the steps of: partitioning the circuit into a plurality of group circuits,

each group circuit includes one or more leaf circuits, wherein each leaf circuit produces a predictable set of output signals with a given set of input signals *(fig.1-3, 5-6 & their description, also col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2);* storing the group circuits in a scheduled event queue in accordance with priority in time which the group circuits need to be simulated *(fig.1-6 & their description, also col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2)*; retrieving from the scheduled event queue a set of group circuits for simulation within a predetermined time period *(fig.1-3,5-6 & their description, also col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2)*; distributing the set of group circuits into a set of predefined event lists, wherein each of the predefined event list stores one or more group circuits of a corresponding event type *(fig.1-3,5-6 & their description, also col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2)*; simulating the one or more group circuits in each of the predefined event list in accordance with a rate of change of signal conditions of each individual group circuit *(fig.1-3,5-6 & their description, also col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2).* Although Tcherniaev et al. does clearly state the term rate of change of signal, he teaches a simulating over certain period of time and obtaining node voltages at specific time (see col.1 line 7-col.5 line 63). Nevertheless, Zhou et al. substantially teaches the term change of signal *(see fig.9 & its description)*. Tcherniaev et al. are analogous art because they are from the same field of endeavor and that the method and apparatus teach by Tcherniaev et al. is similar to that of the Zhou et al. Therefore, it would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the simulation method and system of

Zhou et al. with the hierarchical data circuit simulation of Tcherniaev et al. because Zhou et al. teaches the advantage of producing accuracy results *(col.2 lines 14-41), and* Zhou et al. further teaches a simulation with simplified matrix computations and reduced amount of memory required to perform circuit simulation *(col.2 lines 22-59).*

2.2 With regards to claims 2,13, and 24, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the set of predefined event lists comprise: an active event list for storing group circuits that need to be solved within the predetermined time period *(see Tcherniaev et al. fig.1-5, 8-11 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description);* an isomorphic event list for storing group circuits that need to be solved due to changes in isomorphic behavior of leaf circuits in each of the group circuit *(see Tcherniaev et al. fig.1-5, 8-11 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*; and an adaptive event list for storing group circuits that need to be solved due to changes in connectivity between leaf circuits in each of the group circuit *(see Tcherniaev et al. fig.1-5, 8-11 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description).*

2.3 As per claims 3,14, and 25, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the changes in isomorphic behavior include: changes in isomorphic behavior detected at an output port of a leaf circuit *(see Tcherniaev et al. fig.1-5, 8-11 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-*

col.17 line 2), also see Zhou et al. figures & their description); changes in isomorphic behavior detected at an input port load of a corresponding leaf circuit *(see Tcherniaev et al. fig.1-5, 8-11 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*; and changes in isomorphic behavior detected at a port connectivity interface of a corresponding group circuit *(see Tcherniaev et al. fig.1-5, 8-11 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*.

2.4 Regarding claims 4,15, and 26, the combined teachings of Tcherniaev et al. and Zhou et al. teach that each group circuit stores an event time for indicating priority in time the group circuit need to be solved, and wherein all leaf circuits in the corresponding group circuit share the same event time *(see Tcherniaev et al. fig.1-5, 8-11 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*.

2.5 With regards to claims 5,16, and 27, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the step of simulating comprises: determining a global accepted time by selecting a maximum time among all local accepted times of the one or more group circuits *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*; determining a global current time by selecting a minimum time among all local current times of the one or more group circuits *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their*

description); solving the one or more group circuits in accordance with the global accepted time and the global current time *(see Tcherniaev et al. fig.1-5, 8-13,17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*; and storing solved group circuits to the scheduled event queue in response to the next event time the simulated group circuits need to be simulated *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*.

2.6 As per claims 6,17, and 28, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the local accepted time is the time of last accepted solution of a group circuit *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*.

2.7 Regarding claims 7,18, and 29, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the local current time is the time of a currently calculated solution of a group circuit *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*.

2.8 With regards to claims 8,19, and 30, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the local accepted time of a group circuit is less than the local current time of the corresponding group circuit *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*.

2.9 As per claims 9,20, and 31, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the global accepted time is less than the global current time *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*.

2.10 Regarding claims 10,21, and 32, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the step of simulating further comprises communicating a set of changes in signal conditions from a group circuit to other group circuits via a port connectivity interface *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*.

2.11 Regarding claims 11,22, and 33, Regarding claims 7,18, and 29, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the port connectivity interface comprises: a set of input vectors for referencing to a set of input ports of leaf circuits in receiver group circuits *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*; a set of output vectors for referencing to a set of output ports of leaf circuits in driver group circuits *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description)*; a set of load vectors for referencing to a set of loads of leaf circuits in the driver group circuits *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their*

description); and an array of storage elements for storing information associating the set of loads to the set of input ports *(see Tcherniaev et al. fig.1-5, 8-13, 17 & their description, col.1 line 7-col.5 line 63 and col.13 line 7-col.17 line 2), also see Zhou et al. figures & their description).*

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

3.1 Morgan (U.S. Patent No. 6,083,271) teaches a method and apparatus for specifying multiple power domains in electronic circuit designs.

3.2 Bonitz (U.S. Patent No. 6,237,126) teaches an electrical analysis of integrated circuits.

4. Claims 1-33 are rejected and this action is non-final. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 17, 2006

APL

Paul L. Rodriguez 5/23/06

Primary Examiner
Art Unit 2125 2123